What is claimed is:

1. A signal transmission circuit comprising:

a first signal transmission path for receiving a first input signal, and for outputting a corresponding first output signal which is delayed by a first delay time from the first input signal;

a second signal transmission path for receiving a second input signal, and for outputting a corresponding second temporary signal which is delayed by a second delay time from the second input signal;

an auxiliary signal transmission path for receiving the first input signal, and for outputting a first temporary signal having a third delay associated with the second delay time;

a controlling unit for comparing the first output signal and the first temporary signal to generate an adjustment control signal; and

a controllable delay unit for receiving the adjustment control signal to adjust an internal delay time thereof, and for receiving the second temporary signal for outputting a second output signal which is delayed by the internal delay time from the second temporary signal.

2. The circuit of claim 1, wherein

the auxiliary signal transmission path is a replica of the second signal transmission path.

3. The circuit of claim 1, wherein

the adjustment control signal is such that the first delay time substantially equals the second delay time plus the internal delay time.

4. The circuit of claim 1, wherein

the controllable delay unit is implemented by a voltage controlled delay.

5. The circuit of claim 1, wherein the controllable delay unit comprises:

a plurality of delay branches; and

a multiplexer for selecting, responsive to the adjustment control signal, one of the delay branches.

6. The circuit of claim 1, wherein the controlling unit comprises:

a master variable delay unit adapted to receive the first temporary signal, and having a master internal delay which is controlled by the adjustment control signal; and

a control unit for receiving an output signal of the master variable delay unit and the first output signal to generate the adjustment control signal.

7. The circuit of claim 6, wherein

the master variable delay unit and the controllable delay unit are made identically, and

the master internal delay is controlled to substantially equal the internal delay of the controllable delay unit.

8. The circuit of claim 6, wherein the master variable delay unit comprises:

a plurality of delay branches; and

a multiplexer for selecting, responsive to the adjustment control signal, one of the delay branches.

9. The circuit of claim 6, wherein the control unit comprises:

a phase detector adapted to detect a phase difference between the first output signal and the output signal of the master variable delay unit, and to generate a detect signal responsive to the phase difference.

10. The circuit of claim 9, wherein the master variable delay unit comprises:

a plurality of delay branches; and

a multiplexer for selecting, responsive to the adjustment control signal, one of the delay branches.

11. The circuit of claim 9, wherein

the control unit further includes an electric charge pump unit for generating the adjustment control signal responsive to the detect signal, and

the master variable delay unit and the controllable delay unit are implemented by voltage controlled variable delay units.

12. The circuit of claim 9, wherein

the control unit further includes a register for generating the adjustment control signal responsive to the detect signal, and

the master variable delay unit and the controllable delay unit are implemented by code controlled variable delay units.

13. The circuit of claim 1, wherein

the controlling unit is adapted to generate the adjustment control signal according to a phase difference between the first output signal and the first temporary signal.

14. The circuit of claim 13, wherein

the adjustment control signal has a voltage level proportional to the phase difference according to a first proportionality constant, and

the internal phase delay has a magnitude proportional to the voltage level of the adjustment control signal according to a second proportionality constant.

15. The circuit of claim 14, wherein

the product of the first proportionality constant and the second proportionality constant substantially equals one.

16. The circuit of claim 13, wherein the controlling unit comprises:

a plurality of delay elements, each of which delays the first temporary signal by a predetermined delay time and outputs a delayed output signal;

phase detectors corresponding the plurality of delay elements, each of the phase detectors for outputting phase comparison signals by comparing the phase of

one signal of the output signals of the delay elements with the phase of the first signal transmission path; and

an encoder for receiving each of the phase comparison signals output from the phase detectors and generating the control code.

17. A data latch circuit of a semiconductor device comprising:

a reference signal transmission path for delaying a reference signal by a predetermined first delay time and outputting a delayed reference signal;

first through N-th data transmission paths for delaying first through N-th input data by a predetermined second delay time, respectively, and outputting delayed data of each of the input data;

an auxiliary signal transmission path having delay characteristics identical with those of the first data transmission path, for receiving the reference signal;

a master variable delay unit serially-connected to the auxiliary signal transmission path, and having a delay time which is controlled by a control signal;

first through N-th slave variable delay units serially-connected to the first through N-th data transmission paths, respectively, and having delay times which are controlled by the control signal;

a control unit for receiving an output signal of the master variable delay unit and an output signal of the reference signal transmission path, and for generating the control signal in response thereto; and

first through N-th data latch means for receiving output signals of the first through N-th slave variable delay units, respectively, responsive to the delayed reference signal.

18. The circuit of claim 17, wherein the control unit comprises:

a phase detector adapted to detect a phase difference between the output signal of the reference signal transmission path and the output signal of the master variable delay unit, and to generate a detect signal responsive to the phase difference.

19. The circuit of claim 18, wherein

the control unit further includes an electric charge pump unit for generating the control signal responsive to the detect signal, and

the master variable delay unit and the first through N-th slave variable delay units are voltage controlled variable delay units.

20. The circuit of claim 18, wherein

the control unit further includes a register for generating the control signal responsive to the detect signal, and

the master variable delay unit and the first through N-th slave variable delay units are digital code controlled variable delay units.

21. The circuit of claim 18, wherein

the first through N-th data latch means and the phase detector are flip-flops.

22. A signal transmission method implemented in a signal transmission circuit having first and second signal transmission paths, each of which has different delay characteristics, the method comprising the steps of:

additionally including a auxiliary signal transmission path having delay characteristics identical with the second signal transmission path and a master variable delay unit serially-connected to the auxiliary signal transmission path;

additionally including a slave variable delay unit serially-connected to the second signal transmission path;

inputting a first input signal to the first signal transmission path and the auxiliary signal transmission path, and inputting a second input signal to the second signal transmission path;

generating a control signal corresponding to the phase difference obtained by comparing the phase of an output signal of the first signal transmission path with the phase of an output signal of the master variable delay unit;

controlling the delay time of the master variable delay unit by applying the control signal to the master variable delay unit; and

controlling the delay time of the slave variable delay unit to be identical with the delay time of the master variable delay unit by applying the control signal to the slave variable delay unit.

23. A signal transmission circuit comprising:

a first signal transmission path for receiving a first input signal, and for outputting a corresponding first output signal which is delayed by a first delay time from the first input signal;

a second signal transmission path for receiving a second input signal, and for outputting a corresponding second temporary signal which is delayed by a second delay time from the second input signal;

an auxiliary signal transmission path which is a replica of the second signal transmission path, for receiving the first input signal, and for outputting a first temporary signal which is delayed by the second delay time from the first input signal;

a controlling unit for comparing the first output signal and the first temporary signal to generate an adjustment control signal; and

a controllable delay unit for receiving the adjustment control signal to adjust an internal delay time thereof, and for receiving the second temporary signal for outputting a second output signal which is delayed by the internal delay time from the second temporary signal.

24. A signal transmission circuit comprising:

a first signal transmission path for receiving a first input signal, and for outputting a corresponding first output signal which is delayed by a first delay time from the first input signal;

a second signal transmission path for receiving a second input signal, and for outputting a corresponding second temporary signal which is delayed by a second delay time from the second input signal;

an auxiliary signal transmission path which is a replica of the second signal transmission path, for receiving the first input signal, and for outputting a first

temporary signal which is delayed by the second delay time from the first input signal;

a controlling unit for comparing the first output signal and the first temporary signal to generate an adjustment control signal; and

a controllable delay unit for receiving the adjustment control signal to adjust an internal delay time thereof, and for receiving the second temporary signal for outputting a second output signal which is delayed by the internal delay time from the second temporary signal,

wherein the sum of the second delay time and the internal delay time is controlled to substantially equal the first delay time.

25. A signal transmission circuit comprising:

a first signal transmission path for receiving a first input signal, and for outputting a corresponding first output signal which is delayed by a first delay time from the first input signal;

a second signal transmission path for receiving a second input signal, and for outputting a corresponding second temporary signal which is delayed by a second delay time from the second input signal;

an auxiliary signal transmission path which is a replica of the second signal transmission path, for receiving the first input signal, and for outputting a first temporary signal which is delayed by the second delay time from the first input signal;

a controlling unit comprising a master variable delay unit for receiving the first temporary signal and an adjustment control signal, and a control unit for comparing the output signal of the master variable delay unit and the first output signal, and generating the adjustment control signal; and

a slave variable delay unit for receiving the adjustment control signal to adjust an internal delay time thereof, and for receiving the second temporary signal for outputting a second output signal which is delayed by the internal delay time from the second temporary signal,

wherein the sum of the second delay time and the internal delay time is controlled to substantially equal the first delay time.

26. A signal transmission circuit comprising:

a clock signal transmission path for receiving a clock input signal, and for outputting a corresponding clock output signal which is delayed by a first delay time from the clock input signal;

a data signal transmission path for receiving a data input signal, and for outputting a corresponding data temporary signal which is delayed by a second delay time from the data input signal;

an auxiliary signal transmission path which is a replica of the data signal transmission path, for receiving the clock input signal, and for outputting a clock temporary signal which is delayed by the second delay time from the clock input signal;

a controlling unit for comparing the clock output signal and the clock temporary signal to generate an adjustment control signal; and

a controllable delay unit for receiving the adjustment control signal to adjust an internal delay time thereof, and for receiving the data temporary signal for outputting a data output signal which is delayed by the internal delay time from the data temporary signal.

27. A signal transmission circuit comprising:

a clock signal transmission path for receiving a clock input signal, and for outputting a corresponding clock output signal which is delayed by a first delay time from the clock input signal;

a data signal transmission path for receiving a data input signal, and for outputting a corresponding data temporary signal which is delayed by a second delay time from the data input signal;

an auxiliary signal transmission path which is a replica of the data signal transmission path, for receiving the clock input signal, and for outputting a clock temporary signal which is delayed by the second delay time from the clock input signal;

a controlling unit comprising a master variable delay unit for receiving the clock temporary signal and an adjustment control signal, and a control unit for

comparing the output signal of the master variable delay unit and the clock output signal, and generating the adjustment control signal; and

a slave variable delay unit for receiving the adjustment control signal to adjust an internal delay time thereof, and for receiving the data temporary signal for outputting a data output signal which is delayed by the internal delay time from the data temporary signal.

28. A signal transmission circuit comprising:

a clock signal transmission path for receiving a clock input signal, and for outputting a corresponding clock output signal which is delayed by a first delay time from the clock input signal;

a data signal transmission path for receiving a data input signal, and for outputting a corresponding data temporary signal which is delayed by a second delay time from the data input signal;

an auxiliary signal transmission path which is a replica of the data signal transmission path, for receiving the clock input signal, and for outputting a clock temporary signal which is delayed by the second delay time from the clock input signal;

a controlling unit comprising a first voltage controlled variable delay unit for receiving the clock temporary signal and an adjustment control signal, and a phase detector for detecting a phase difference between the output signal of the first voltage controlled variable delay unit and the clock output signal and generating a detect signal responsive to the phase difference, and an electric charge pump unit for generating the adjustment control signal responsive to the detect signal; and

a second voltage controlled variable delay unit for receiving the adjustment control signal to adjust an internal delay time thereof, and for receiving the data temporary signal for outputting a data output signal which is delayed by the internal delay time from the data temporary signal,

wherein the sum of the second delay time and the internal delay time is substantially controlled to equal the first delay time.

29. A signal transmission circuit comprising:

a clock signal transmission path for receiving a clock input signal, and for outputting a corresponding clock output signal which is delayed by a first delay time from the clock input signal;

a data signal transmission path for receiving a data input signal, and for outputting a corresponding data temporary signal which is delayed by a second delay time from the data input signal;

an auxiliary signal transmission path which is a replica of the data signal transmission path, for receiving the clock input signal, and for outputting a clock temporary signal which is delayed by the second delay time from the clock input signal;

a controlling unit comprising a first digital code controlled variable delay unit for receiving the clock temporary signal and a digital code signal, and a phase detector for detecting a phase difference between the output signal of the first digital code controlled variable delay unit and the clock output signal and generating a detect signal responsive to the phase difference, and a register for generating the digital code signal responsive to the detect signal; and

a second digital code controlled variable delay unit for receiving the digital code signal to adjust an internal delay time thereof, and for receiving the data temporary signal for outputting a data output signal which is delayed by the internal delay time from the data temporary signal,

wherein the sum of the second delay time and the internal delay time is controlled to substantially equal the first delay time.